translation lookaside buffer (TLB) coherency" as the title indicates. Since coherency between memory systems and coherency of TLBs are different, the Applicant respectfully requests withdrawal of all rejections.

Chang's invention has been designed to solve a TLB coherence problem (Col. 7, Lines 58-62). A TLB is a high-speed translation buffer that facilitates the translation from a "virtual" address (VA) to a "physical" address (PA). As a result, consistency among multiple TLBs refers to the requirement that all TLBs "must" map the same virtual address to the same physical address. Specifically, if processors P0 and P1 issue memory accesses with the same virtual address, TLB0 and TLB1 ought to produce the same physical address. Otherwise, the system will not function correctly because processors that issue reads and writes to the same address would touch different memory location.

Because all TLBs must be maintained consistently for a given VA to PA translation, when a processor attempts to modify its own TLB the processor must inform all other processors about the change. *Importantly, the initiating processor cannot commit the change until all other processors have responded (acknowledged) the request.* This is clearly presented by the protocol in Chang's invention:

1. The initiating processor broadcasts a TLB invalidation message to all other processors, then waits for responses from the other processors (e.g. Col. 7, Lines 39-48);
2. Upon receiving a TLB invalidation command, the receiving processor either acknowledges the command or asks the initiating processor to retry (e.g. Col. 9, Lines 4-9); and
3. The initiating processor will collect acknowledgements from all other processors, and retry the request if needed (e.g. Col. 9, Lines 41-63).

Thus, Chang maintains consistency among TLBs in a *synchronous* manner. Because the initiating processor cannot proceed with the change, it is impossible for two processors to observe different VA to PA mappings.

In contrast, the present invention is designed to deal with "accessing memory in a multiprocessor system." Because both problems are relevant to consistency among multiple copies

of the same data object, one could easily mistake that both are identical problems. But, for at least the reasons outlined below, differences exist.

These differences are reflected in the claims. Claim 1 refers to "a request for a block of data to one or more other processors and memory." Independent claim 9 refers to a system of "two or more processors, each in communication with a shared memory via a memory controller; the processors ... issuing a request for a block of data." Independent claim 19 refers to a system of shared memory that is capable of, "issuing a request for a block of data."

The Office Action equates Chang's checking on the valid/invalid state of the block of data and issuing an instruction regarding invalidation with the claimed request for "a block of data" itself. The Applicant respectfully disagrees for two reasons. First, an instruction to change the state associated with a block of data, as it appears is taught in Chang, is not the same thing as "a request for a block of data," as is taught in the present invention. Second, the change of state within a TLB, as it appears is taught in Chang, is not the same as "a request for a block of data," as is taught in the present invention. For at least these reasons, the Applicant requests that the §102 rejection of claims 1, 9 and 19 be withdrawn.

Should the Examiner consider rejecting the claims under §103 in view of Chang, such a rejection would be inappropriate. As explained above, Chang fails to teach or suggest "a request for a block of data" from memory systems associated with multiprocessor systems. Furthermore, Chang's disclosure addresses a different problem from the present invention, and one skilled in the art would not look to Chang for teaching or guidance.

For at least the foregoing reasons, independent claims 1, 9, and 19 are allowable over the prior art of record. All claims, 2-8, 10-18, and 20 depend from one of the independent claims and are therefore allowable for at least the same reasons.

Conclusion

As all of the outstanding rejections have been traversed and all of the claims are believed to be in condition for allowance, the Applicants respectfully request issuance of a Notice of

Allowability. If the undersigned attorney can assist in any matters regarding examination of this application, the Examiner is encouraged to call at the number listed below.

Respectfully submitted,

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